National Semiconductor

February 2001

CLC440
High Speed, Low Power, Voltage Feedback Op Amp

General Description

The CLC440 is a wideband, low power, voltage feedback op amp that offers 750MHz unity-gain bandwidth, 1500V/µs slew rate, and 90mA output current. For video applications, the CLC440 sets new standards for voltage feedback monolithics by offering the impressive combination of 0.015% differential gain and 0.025° differential phase errors while dissipating a mere 70mW.

The CLC440 incorporates the proven properties of Comlinear's current feedback amplifiers (high bandwidth, fast slewing, etc.) into a "classical" voltage feedback architecture. This amplifier possesses truly differential and fully symmetrical inputs both having a high 900kΩ impedance with matched low input bias currents. Furthermore, since the CLC440 incorporates voltage feedback, a specific R_f is not required for stability. This flexibility in choosing R_f allows for numerous applications in wideband filtering and integration.

Unlike several other high speed voltage feedback op amps, the CLC440 operates with a wide range of dual or single supplies allowing for use in a multitude of applications with limited supply availability. The CLC440's low 3.5nV/$\sqrt{Hz}$ (e_n) and 2.5pA/ $\sqrt{Hz}$ (i_n) noise sets a very low noise floor.

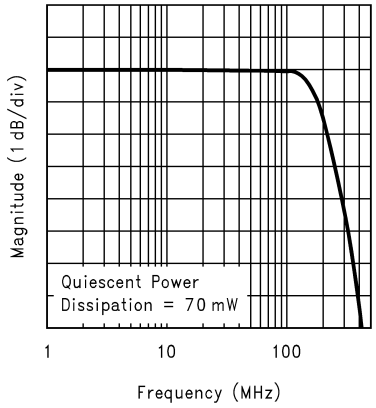
Features

- Unity-gain stable
- High unity-gain bandwidth: 750MHz
- Ultra low differential gain: 0.015%
- Very low differential phase: 0.025°
- Low power: 70mW
- Extremely fast slew rate: 1500V/µs
- High output current: 90mA
- Low noise: 3.5nV/$\sqrt{Hz}$
- Dual ±2.5V to ±6V or single 5V to 12V supplies

Applications

- Professional video
- Graphics workstations
- Test equipment
- Video switching & routing
- Communications
- Medical imaging
- A/D drivers
- Photo diode transimpedance amplifiers
- Improved replacement for CLC420 or OPA620

Frequency Response (A_V = +2V/V)



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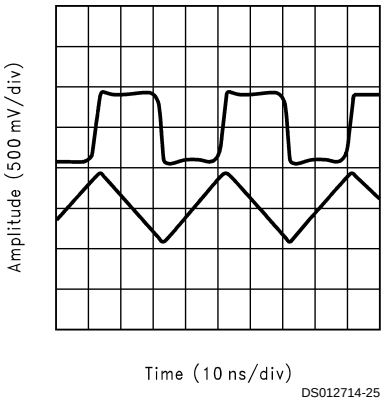
Generator Waveforms



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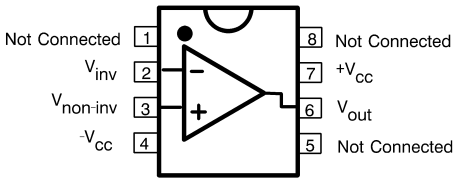
Connection Diagram



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Pinout
DIP & SOIC

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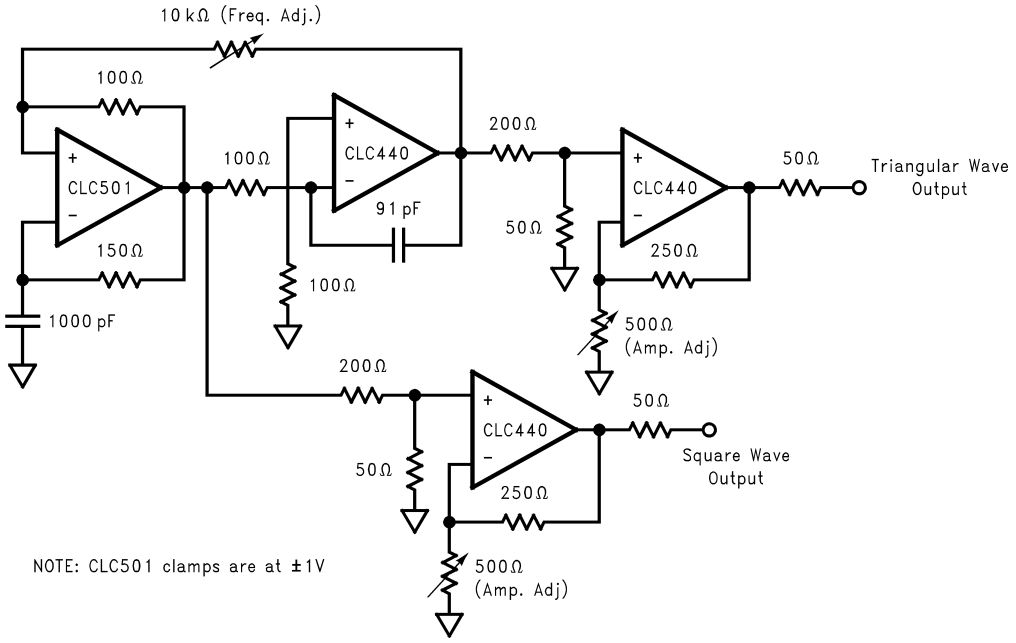
Typical Application



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Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	−40˚C to +85˚C	CLC440AJP	CLC440AJP	N08E
8-pin plastic SOIC	−40˚C to +85˚C	CLC440AJE	CLC440AJE	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	±6V
I_{OUT} is short circuit protected to ground	
Common Mode Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (soldering, 10 sec)	+300˚C
ESD rating (human body model)	<1000V

Operating Ratings

Thermal Resistance		
Package	(θ_{JC})	(θ_{JA})
MDIP	70˚C/W	125˚C/W
SOIC	60˚C/W	140˚C/W

Electrical Characteristics

A_V = +2, R_f = R_g = 250Ω; V_{CC} = ±5V, R_L = 100Ω unless specified.

Symbol	Parameter	Conditions	Typ	Min/Max (Note 2)			Units
Ambient Temperature		CLC440IN	+25˚C	+25˚C	0 to 70˚C	−40 to 85˚C	
Frequency Domain Response							
	−3dB Bandwidth A_V = +2	V_{OUT} <0.2V_{PP}	260	165	165	135	MHz
		V_{OUT}<4.0V_{PP}	190	150	135	130	MHz
	−3dB Bandwidth A_V = +1	V_{OUT} <0.2V_{PP}	750				MHz
	Gain Bandwidth Product	V_{OUT} <0.2V_{PP}	230				MHz
	Gain Flatness	V_{OUT}< 2.0V_{PP}, DC to 75MHz	0.05	0.15	0.20	0.20	dB
	Linear Phase Deviation	V_{OUT}< 2.0V_{PP}, DC to 75MHz	0.8	1.2	1.5	1.5	deg
	Differential Gain	R_L=150Ω, 4.43MHz	0.015	0.03	0.04	0.04	%
	Differential Phase	R_L=150Ω, 4.43MHz	0.025	0.05	0.06	0.06	deg
Time Domain Response							
	Rise and Fall Time	2V step	1.5	2.0	2.2	2.5	ns
		4V step	3.2	4.2	4.5	5.0	ns
	Settling Time to ±0.05%	2V step	10	14	16	16	ns
	Overshoot	4V step	7	13	13	13	%
	Slew Rate	4V step, ±0.5V crossing	1500	900	750	600	V/µs
Distortion And Noise Response							
	2nd Harmonic Distortion	2V_{PP}, 5MHz	−64	−59	−59	−59	dBc
		2V_{PP}, 20MHz	−52	−46	−46	−46	dBc
	3rd Harmonic Distortion	2V_{PP}, 5MHz	−70	−65	−64	−64	dBc
		2V_{PP}, 20MHz	−51	−45	−43	−43	dBc
	Equivalent Input Noise						
	Voltage	>1MHz	3.5	4.5	5.0	5.0	nV/$\sqrt{Hz}$
	Current	>1MHz	2.5	3.5	4.0	4.0	pA/$\sqrt{Hz}$
Static DC Performance							
	Input Offset Voltage (Note 3)		1.0	3.0	3.5	4.0	mV
	Average Drift		5.0	-	10	10	µV/˚C
	Input Bias Current (Note 3)		10	30	35	40	µA
	Average Drift		30	-	50	60	nA/˚C
	Input Offset Current (Note 3)		0.5	2.0	2.0	3.0	µA
	Average Drift		3.0	-	10	10	nA/˚C
	Power Supply Rejection Ratio	DC	65	58	58	58	dB
	Common Mode Rejection Ratio	DC	80	65	60	60	dB
	Supply Current (Note 3)	R_L = ∞	7.0	7.5	8.0	8.0	mA
Miscellaneous Performance							
	Input Resistance	Common-Mode	900	500	400	300	kΩ

Electrical Characteristics (Continued)

A_V = +2, R_f = R_g = 250Ω; V_{CC} = ±5V, R_L = 100Ω unless specified.

Symbol	Parameter	Conditions	Typ	Min/Max (Note 2)			Units
Miscellaneous Performance							
	Input Capacitance	Common-Mode	1.2	2.0	2.0	2.0	pF
		Differential-Mode	0.5	1.0	1.0	1.0	pF
	Input Voltage Range	Common-Mode	±3.0	±2.8	±2.7	±2.7	V
	Output Voltage Range	R_L = 100Ω	±2.5	±2.3	±2.2	±2.2	V
	Output Voltage Range	R_L = ∞	±3.0	±2.8	±2.7	±2.7	V
	Output Current		±80	±72	±65	±45	mA

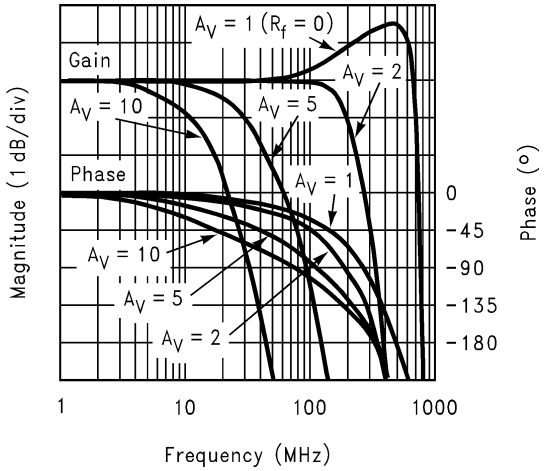
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: AJ-level: spec. is 100% tested at +25°C.

Typical Performance Characteristics

Non-Inverting Frequency Response



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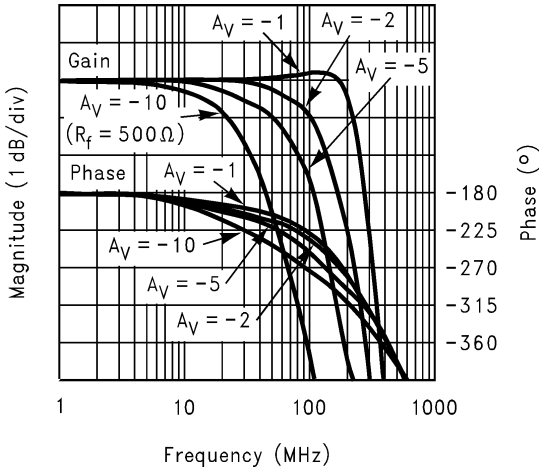
Inverting Frequency Response



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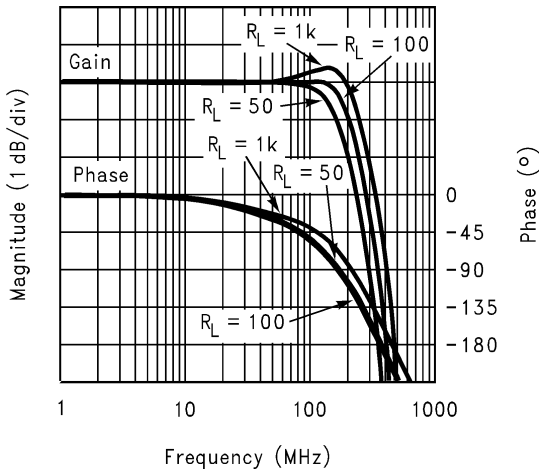
Frequency Response vs. Load



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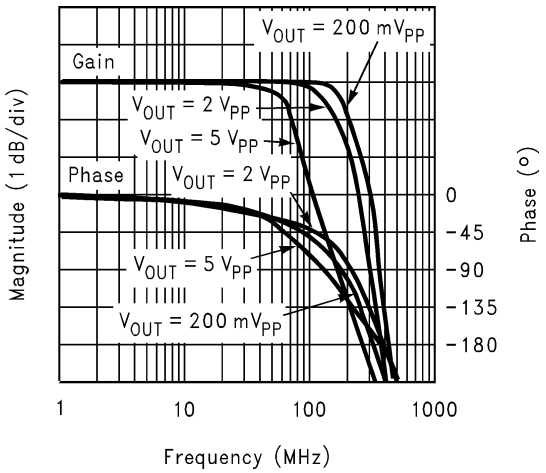
Frequency Response vs. V_{OUT}



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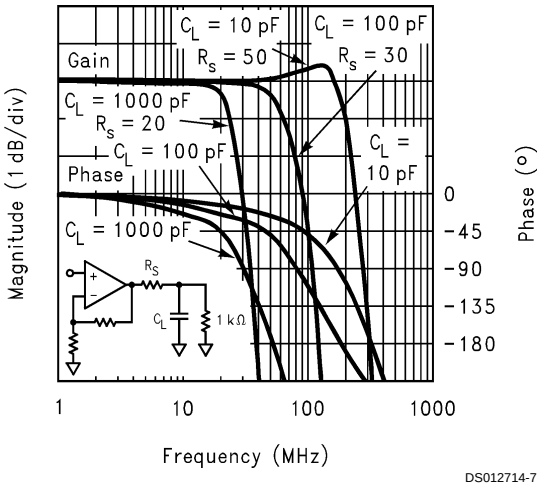
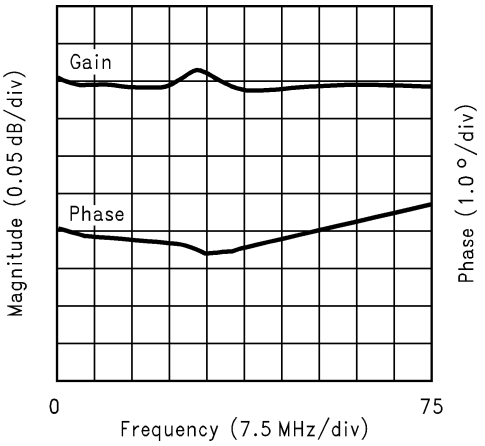
Typical Performance Characteristics (Continued)

Frequency Response vs. Capacitive Load



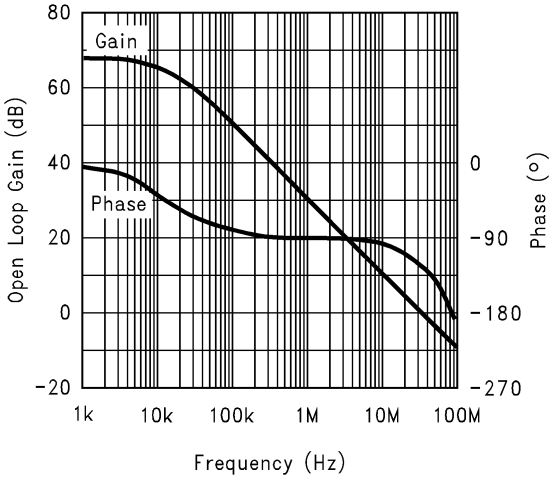
DS012714-7

Gain Flatness and Linear Phase



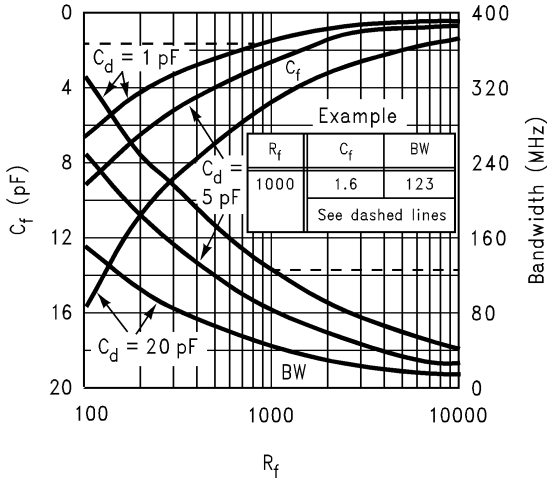
DS012714-41

Open Loop Gain and Phase



DS012714-8

BW vs. Gain for Transimpedance Configuration



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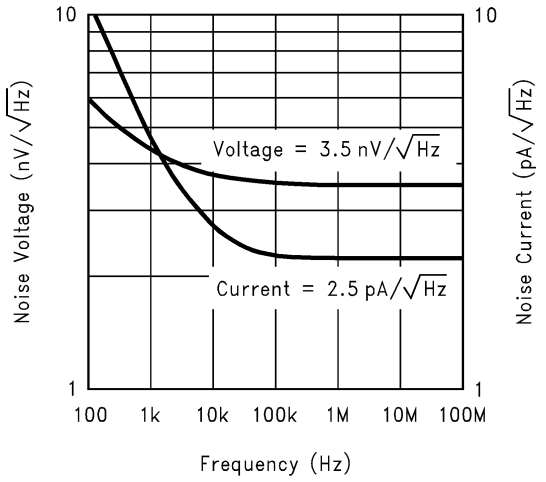
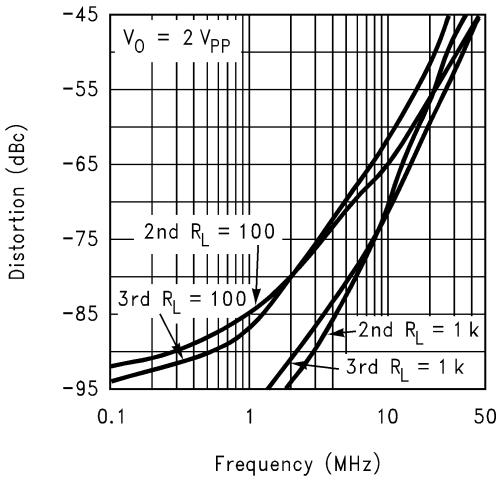
Equivalent Input Noise



DS012714-10

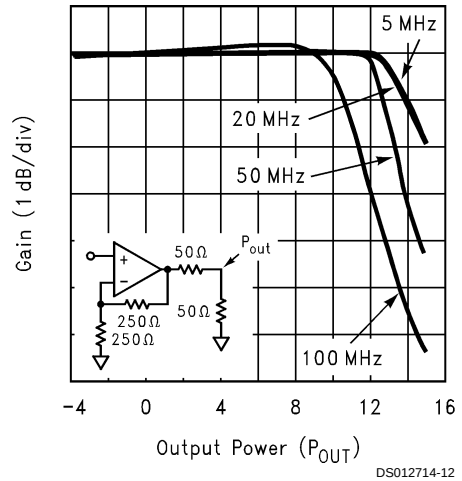
Harmonic Distortion vs. Frequency



DS012714-11

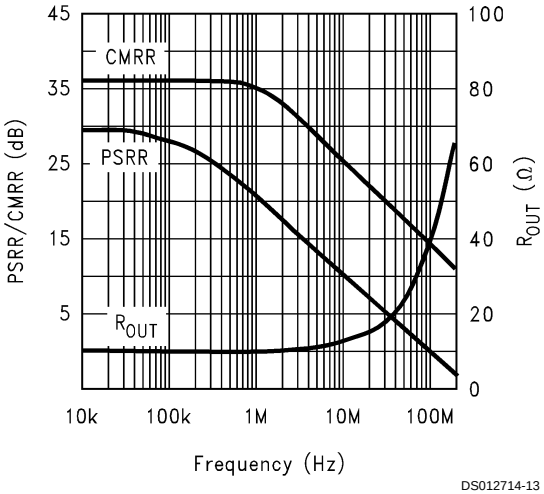
Typical Performance Characteristics (Continued)

1dB Compression



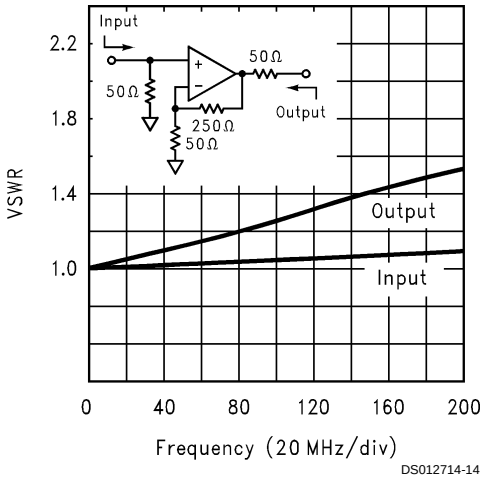
DS012714-12

PSRR, CMRR, and Closed Loop R_{OUT}



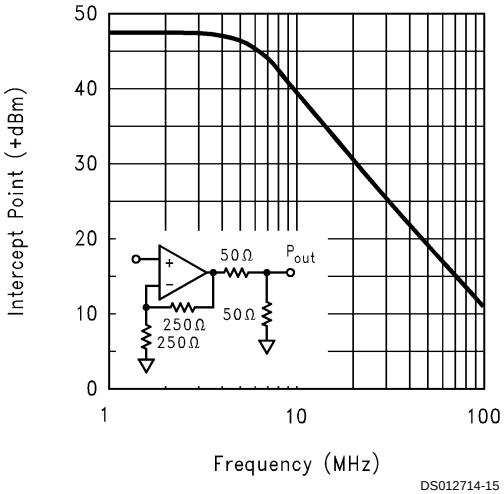
DS012714-13

Input and Output VGWR



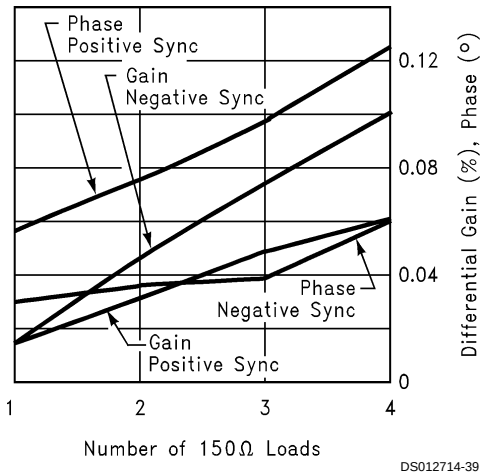
DS012714-14

2-Tone, 3rd Order Intermodulation Intercept



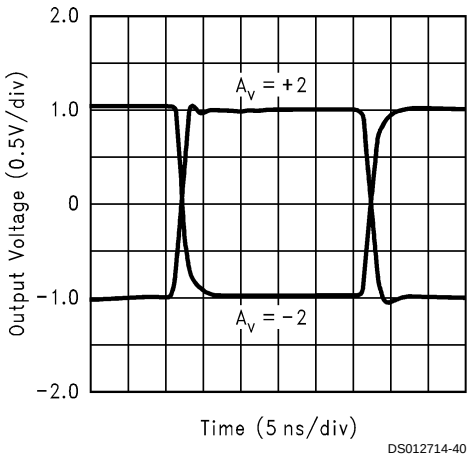
DS012714-15

Differential Gain and Phase



DS012714-39

Pulse Response



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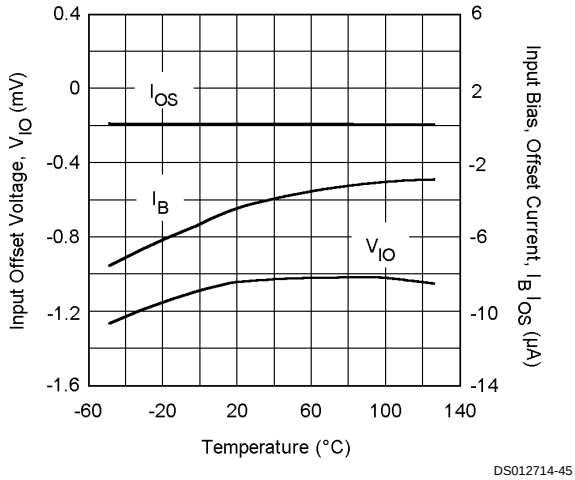
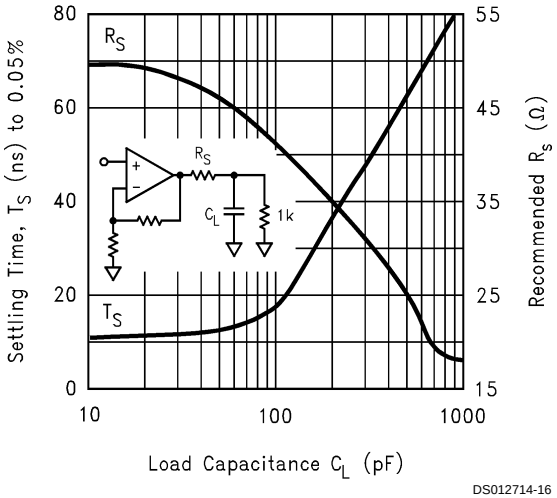
Typical Performance Characteristics (Continued)

Typical DC Errors vs. Temperature



DS012714-45

0.05% Settling Time vs. Capacitive Load



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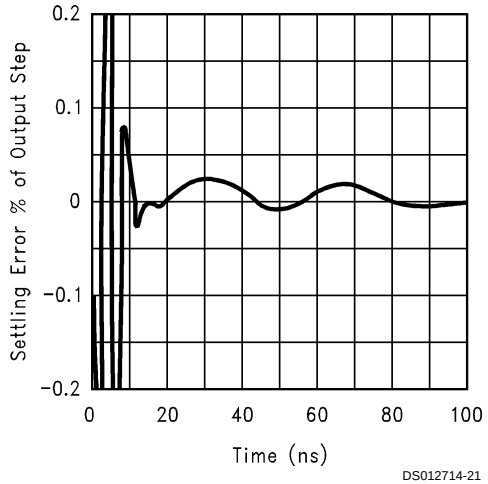
Short Term Settling Time



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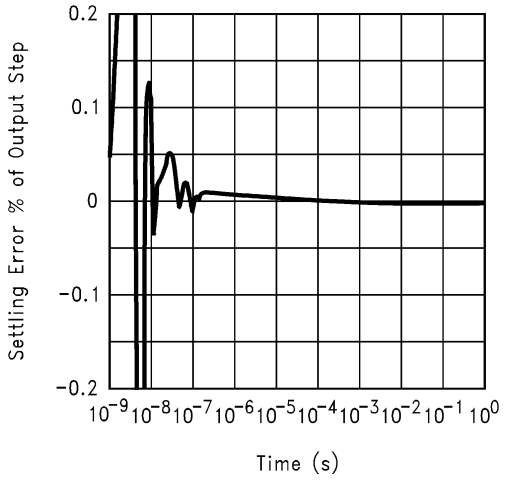
Long Term Settling Time



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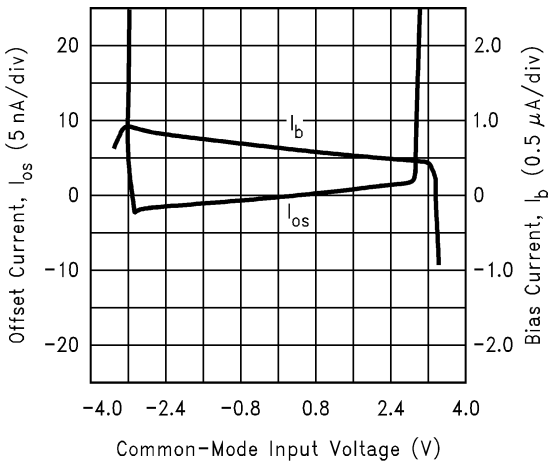
I_B and I_{OS} vs. Common-Mode Voltage



DS012714-23

Application Division

General Design Equations

The CLC440 is a unity gain stable voltage feedback amplifier. The matched input bias currents track well over temperature. This allows the DC offset to be minimized by matching the impedance seen by both inputs.

Gain

The non-inverting and inverting gain equations for the CLC440 are as follows:

$$\text{NON-INVERTING GAIN: } 1 + \frac{R_f}{R_g}$$

$$\text{INVERTING GAIN: } -\frac{R_f}{R_g}$$

Gain Bandwidth Product

The CLC440 is a voltage feedback amplifier, whose closed-loop bandwidth is approximately equal to the gain-bandwidth product (GBP) divided by the gain (Av). For gains greater than 5, Av sets the closed-loop bandwidth of the CLC440.

$$\text{CLOSE LOOP BANDWIDTH} = \frac{GBP}{A_V}$$

$$A_V = \frac{(R_f = R_g)}{R_g}$$

$$GBP = 230MHz$$

For gains less than 5, refer to the frequency response plots to determine maximum bandwidth.

Output Drive and Settling Time Performance

The CLC440 has large output current capability. The 90mA of output current makes the CLC440 an excellent choice for applications such as:

- Video Line Drivers
- Distribution Amplifiers

When driving a capacitive load or coaxial cable, include a series resistance R_s to back match or improve settling time. Refer to the “Settling Time vs. Capacitive Load” plot in the typical performance section to determine the recommended resistance for various capacitive loads.

When driving resistive loads of under 500Ω, settling time performance diminishes. This degradation occurs because a small change in voltage on the output causes a large change of current in the power supplies. This current creates ringing on the power supplies. A small resistor will dampen this effect if placed in series with 6.8µF bypass capacitor.

Noise Figure

Noise Figure (NF) is a measure of noise degradation caused by an amplifier.

$$NF = 10LOG\left[\frac{S_i/N_i}{S_o/N_o}\right] = 10LOG\left[\frac{e_{ni}^2}{e_t^2}\right]$$

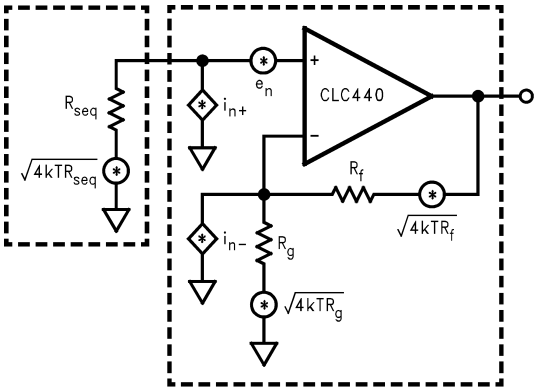
where,

e_{ni} = Total Equivalent Input Noise Density Due to the Amplifier

e_t = Thermal Voltage Noise ($\sqrt{4kTR_{seq}}$)

Figure 1 shows the noise model for the non-inverting amplifier configuration. The model includes all of the following noise sources:

- Input voltage noise (e_n)
- Input current noise ($i_n=i_{n+}=i_{n-}$)
- Thermal Voltage Noise (e_t) associated with each external resistor



$R_{seq} = R_s$ for Unterminated Systems

$R_{seq} = R_s$ II R_T for Terminated Systems

DS012714-30

FIGURE 1. Non-Inverting Amplifier Noise Model

The total equivalent input noise density is calculated by using the noise model shown. Equations 1 and 2 represent the noise equation and the resulting equation for noise figure.

$$e_{ni} = \sqrt{e_n^2 + i_n^2\left(R_{seq}^2 + (R_f \| R_g)^2\right) + 4kTR_{seq} + 4kT(R_f \| R_g)} \quad (1)$$

$$NF = 10LOG\left(\frac{e_n^2 + i_n^2\left(R_{seq}^2 + (R_f \| R_g)^2\right) + 4kTR_{seq} + 4kT(R_f \| R_g)}{4kTR_{seq}}\right) \quad (2)$$

The noise figure is related to the equivalent source resistance (R_{seq}) and the parallel combination of R_f and R_g. To minimize noise figure, the following steps are recommended:

- Minimize $R_f \| R_g$
- Choose the optimum R_s (R_{OPT})
- R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \cong \frac{e_n}{i_n}$$

Figure 2 is a plot of NF vs. R_s with R_f= 0, R_g=∞ (A_v=+1). The NF curves for both Unterminated and Terminated systems are shown. The Terminated curve assumes R_s= R_T. The table indicates the NF for various source resistances including R_s= R_{OPT}.

Application Division (Continued)

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC440 (CLC730055-DIP, CLC730060-SOIC) and suggests their use as a guide for high frequency layout and as an aid in device testing and characterization.

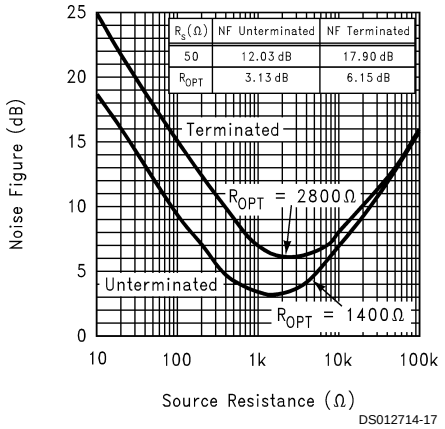


FIGURE 2. Noise Figure vs. Source Resistance

These boards were laid out for optimum, high-speed performance. The ground plane was removed near the input and output pins to reduce parasitic capacitance. And all trace lengths were minimized to reduce series inductances.

Supply bypassing is required for the amplifiers performance. The bypass capacitors provide a low impedance return current path at the supply pins. They also provide high frequency filtering on the power supply traces. 6.8µF tantalum, 0.01µF ceramic, and 500pF ceramic capacitors are recommended on both supplies. Place the 6.8µF capacitors within 0.75 inches of the power pins, and the 0.01µF and 500pF capacitors less than 0.1 inches from the power pins.

Dip sockets add parasitic capacitance and inductance which can cause peaking in the frequency response and overshoot in the time domain response. If sockets are necessary, flush-mount socket pins are recommended. The device holes in the 730055 evaluation board are sized for Cambion P/N 450-2598 socket pins, or their functional equivalent.

Transimpedance Amplifier

The low 2.5pA/$\sqrt{Hz}$ input current noise and unity gain stability make the CLC440 an excellent choice for transimpedance applications. *Figure 3* illustrates a low noise transimpedance amplifier that is commonly implemented with photo diodes. R_f sets the transimpedance gain. The photo diode current multiplied by R_f determines the output voltage.

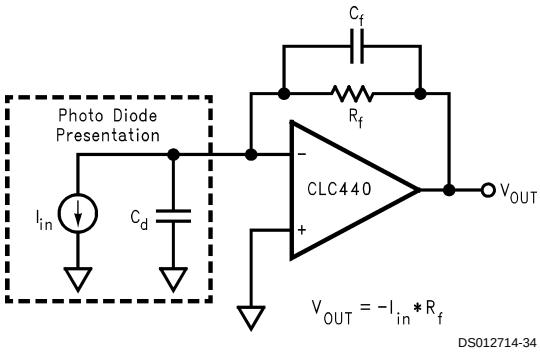


FIGURE 3. Transimpedance Amplifier Configuration

The capacitances are defined as:

- C_{in} = Internal Input Capacitance of the CLC440 (typ 1.2pF)
- C_d = Equivalent Diode Capacitance
- C_f = Feedback Capacitance

The transimpedance plot in the typical performance section provides the recommended C_f and expected bandwidth for different gains and diode capacitances. The feedback capacitances indicated on the plot give optimum gain flatness and stability. If a smaller capacitance is used, then peaking will occur. The frequency response shown in *Figure 4* illustrates the influence of the feedback capacitance on gain flatness.

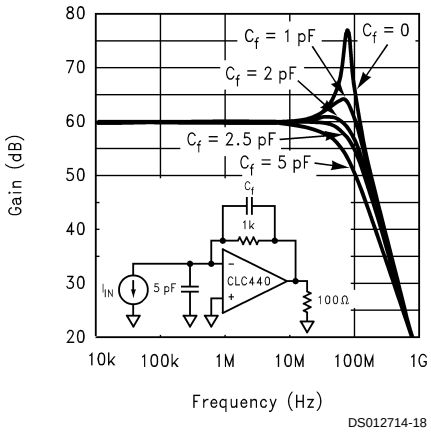


FIGURE 4. Transimpedance Amplifier Frequency Response

The total input current noise density (i_{ni}) for the basic transimpedance configuration is shown in Equation 3. The plot of current noise density versus feedback resistance is shown in *Figure 5*.

Application Division (Continued)

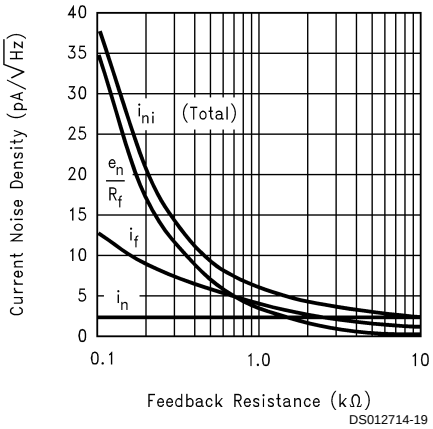


FIGURE 5. Current Noise Density vs. Feedback Resistance

$$i_{ni} = \sqrt{i_n + \left[\frac{e_n^2}{R_f}\right]^2 + \frac{4kT}{R_f}} \quad (3)$$

Rectifier

The large bandwidth of the CLC440 allows for high speed rectification. A common rectifier topology is shown in *Figure 6*. R_1 and R_2 set the gain of the rectifier. V_{OUT} for a 5MHz, $2V_{pp}$ sinusoidal input is shown in *Figure 7*.

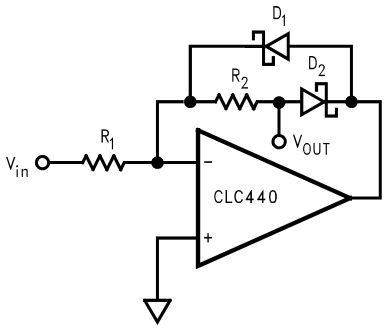


FIGURE 6. Recitifier Topology

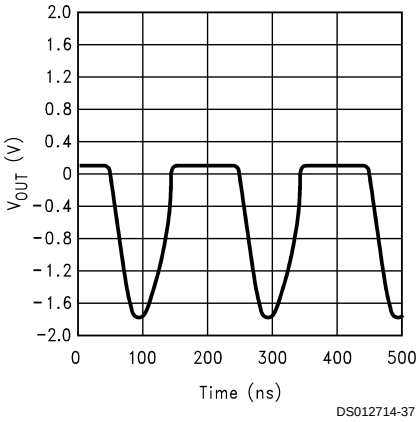


FIGURE 7. Rectifier Output

Tunable Low Pass Filter

The center frequency of the low pass filter (LPF) can be adjusted by varying the CLC522 gain control voltage, V_g.

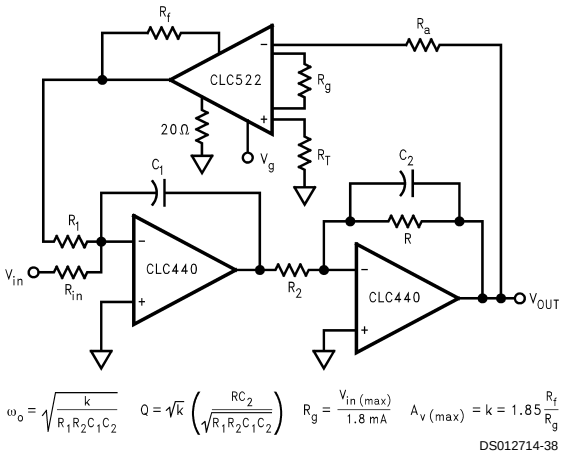
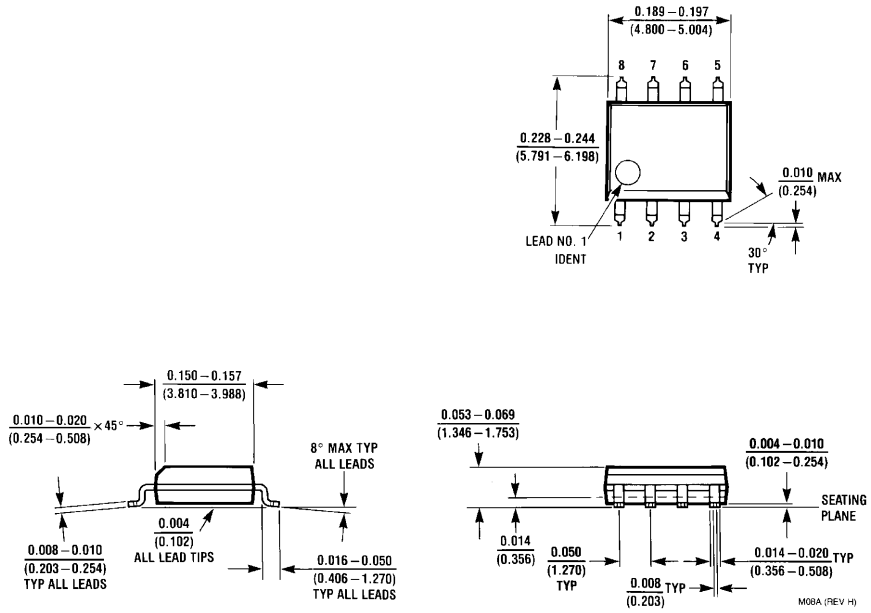
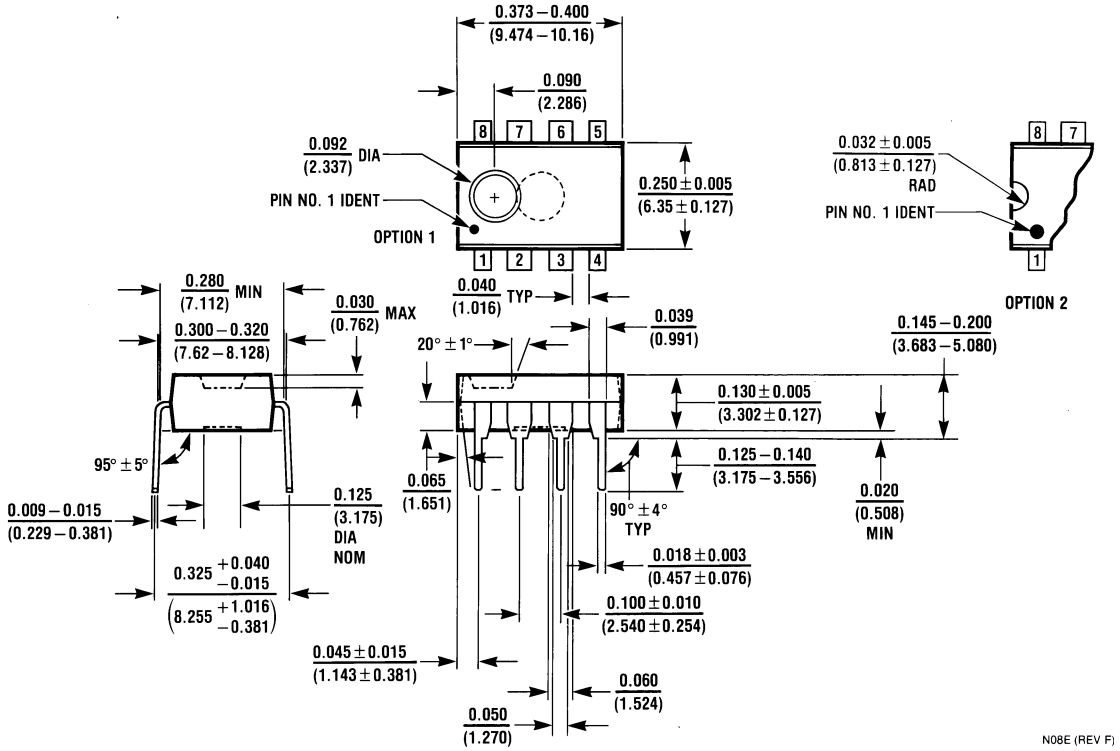


FIGURE 8. Tunable Low Pass Filter

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



8-Pin MDIP
NS Package Number N08E

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